IN THE CLAIMS:

The following listing of claims will replace all prior versions and listings of claims in this application:

Claims 1 – 30 (Cancelled)

31. (New) A method of manufacturing a semiconductor device comprising the steps of:

(a) forming rectangular first electrode pads having a side length of 10 μm or shorter and comprised of an uppermost layer wiring in a scribe region and forming a bonding pad comprised of said uppermost layer wiring in a product circuit region;

(b) forming a protection film on an upper layer of said uppermost layer wiring; and

(c) partially exposing a surface of said bonding pad by removing a predetermined part of said protection film,

wherein said uppermost layer wiring is formed by depositing a conductive body and them patterning by a lithography method.

32. (New) The method of manufacturing a semiconductor device according to claim 31,

wherein said step (a) includes the step of forming second electrode pads having a side length of 20 μm or longer and comprised of said uppermost layer wiring in said scribe region, and said step (c) includes the step of partially exposing a surface of said second electrode pad.

33. (New) A method of manufacturing a semiconductor device comprising the steps of:

(a) sequentially forming a first insulating film, a stopper insulating film, and a second insulating film on a semiconductor substrate;

(b) forming a connection hole in said first insulating film and forming a wiring trench in said stopper insulating film and said second insulating film;

(c) burying a conductor film in said connection hole and said wiring trench and removing said conductor film in a region outside said connection hole and said wiring trench by a CMP method, thereby forming a first electrode pad formed together with a connection member in a first scribe region;

(d) forming a protection film on an upper layer of said first electrode pad; and

(e) removing said protection film and said second insulating film in said first scribe region with said stopper insulating film used as an etching stopper layer, thereby exposing said first electrode pad.

34. (New) The method of manufacturing a semiconductor device according to claim 33,

wherein said step (c) includes the step of forming a bonding pad formed together with a connection member in a product circuit region, said step (d) includes the step of forming a protection film on an upper layer of said bonding pad, and said step (e) includes the step of partially exposing a surface of said bonding pad by removing a predetermined part of said protection film in said product circuit region.

35. (New) The method of manufacturing a semiconductor device according to claim 33,

wherein said step (c) includes the step of forming a second electrode pad formed together with a connection member in a second scribe region, and forming a bonding pad formed together with a connection member in a product circuit region, said step (d) includes the step of forming a protection film on an upper layer of said second electrode pad and said bonding pad, and said step (e) includes the step of removing a predetermined part of said protection film in said second scribe region, thereby partially exposing a surface of said second electrode pad, and further removing a predetermined part of said protection film in said product circuit region, thereby partially exposing a surface of said bonding pad.

36. (New) A method of manufacturing a semiconductor device, comprising the steps of:

(a) forming rectangular first electrode pads having a side length of 0.5 μm or shorter and comprised of an uppermost layer wiring in a scribe region and forming a bonding pad comprised of said uppermost layer wiring in a product circuit region;

(b) forming a protection film on an upper layer of said uppermost layer wiring; and

(c) partially exposing a surface of said bonding pad by removing a predetermined part of said protection film,

wherein said uppermost layer wiring is formed by depositing a conductive body and then patterning by a lithography method,

wherein a plurality of TEGs provided with said first electrode pads are formed in said scribe region, and

wherein, after partially exposing the surface of said first electrode pad by removing said protection film on said first electrode pad, a probe having a tip radius of curvature of about 0.05 μm to 0.8 μm is contacted to said first electrode pad, and then said TEG is measured.

37. (New) A method of manufacturing a semiconductor device, comprising the steps of:

(a) forming rectangular first electrode pads having a side length of 1 μm or shorter and comprised of an uppermost layer wiring in a scribe region and forming a bonding pad comprised of said uppermost layer wiring in a product circuit region;

(b) forming a protection film on an upper layer of said uppermost layer wiring; and

(b) partially exposing a surface of said bonding pad by removing a predetermined part of said protection film,

wherein said uppermost layer wiring is formed by depositing a conductive body and then patterning by a lithography method,

wherein a plurality of TEGs provided with said first electrode pads are formed in said scribe region, and

wherein, after partially exposing the surface of said first electrode pad by removing said protection film on said first electrode pad, a probe having a tip radius of curvature of about 0.05 μm to 0.8 μm is contacted to said first electrode pad, and then said TEG is measured.

38. (New) A method of manufacturing a semiconductor device comprising the steps of:

(a) forming rectangular first electrode pads having a side length of 10 μm or shorter and comprised of an uppermost layer wiring in a scribe region and forming a bonding pad comprised of said uppermost layer wiring in a product circuit region;

(b) forming a protection film on an upper layer of said uppermost layer wiring; and

(c) partially exposing a surface of said bonding pad and a surface of said second electrode pad by removing a predetermined part of said protection film,

wherein said uppermost layer wiring is formed by depositing a conductive body and then patterning by a lithography method,

a plurality of TEGs provided with said first electrode pads and said second electrode pads are formed in said scribe region, and

after partially exposing the surface of said first electrode pad by removing said protection film on said first electrode pad, a probe having a tip radius of curvature of about 0.05 μm to 0.8 μm is contacted to said fist electrode pad, and then said TEG is measured.

39. (New) A method of manufacturing a semiconductor device, comprising the steps of:

(a) forming rectangular first electrode pads having a side length of 10 μm or shorter and rectangular second electrode pads having a side length of 20 μm or shorter each comprised of an uppermost layer wiring in a scribe region and forming a bonding pad comprised of said uppermost layer wiring in a product circuit region;

(b) forming a protection film on an upper layer of said uppermost layer wiring; and

(c) partially exposing a surface of said bonding pad and a surface of said second electrode pad by removing a predetermined part of said protection film,

wherein said uppermost layer wiring is formed by depositing a conductive body and then patterning by a lithography method,

a plurality of TEGs provided with said first electrode pads and said second electrode pads are formed in said scribe region, and

after partially exposing the surface of said first electrode pad by removing said protection film on aid first electrode pad, a probe having a tip radius of curvature of about 0.05 μm to 0.8 μm is contacted to aid first electrode pad, and then said TEG is measured.

40. (New) The method of manufacturing a semiconductor device according to claim 38,

wherein a plurality of TEGs provided with rectangular second electrode pads having a side length of 20 μm or longer and comprised of said uppermost layer wiring are also formed in the scribe region.

41. (New) The method of manufacturing a semiconductor device according to claim 38,

wherein said first electrode pad is set formed so that the length of one side thereof is not longer than the dimension obtained by adding the diameter of a connection hole between said first electrode pad and the underlying wiring and the length of an alignment margin between said first electrode pad and said connection hole.

42. (New) The method of manufacturing a semiconductor device according to claim 38,

wherein said first electrode pad is formed so that the length of one side thereof is about four-thirds of the diameter of a connection hole between said first electrode pad and the underlying wiring.

43. (New) The method of manufacturing a semiconductor device according to claim 38,

wherein the surface of said first electrode pad is exposed in an island shape.

44. (New) The method of manufacturing a semiconductor device according to claim 38,

wherein said protection film on said first electrode pad is removed by a focused ion beam method or a selective etching method.

45. (New) The method of manufacturing a semiconductor device according to claim 39,

wherein said second electrode pad is connected commonly to the plurality of TEGs.

46. (New) A method of manufacturing a semiconductor device, comprising the steps of:

(a) forming rectangular first electrode pads having a side length of 10 μm or shorter and rectangular second electrode pads having a side length of 20 μm or

shorter each comprised of an uppermost layer wiring in a scribe region and forming a bonding pad comprised of said uppermost layer wiring in a product circuit region;

(b) forming a protection film on an upper layer of said uppermost layer wiring; and

(c) partially exposing a surface of said bonding pad and a surface of said second electrode pad by removing a predetermined part of said protection film,

wherein said uppermost layer wiring is formed by depositing a conductive body and then patterning by a lithography method,

a plurality of TEGs provided with said first electrode pads and a plurality of TEGs provided with said second electrode pads are formed in said scribe region, and

after partially exposing the surface of said first electrode pad by removing said protection film on said first electrode pad, a probe having a tip radius of curvature of about 0.05 μm to 0.8 μm is contacted to said first electrode pad, and then said TEG is measured.

47. (New) The method of manufacturing a semiconductor device according to claim 46,

wherein said second electrode pad is connected commonly to the plurality of TEGs.

48. (New) A method of manufacturing a semiconductor device comprising the steps of:

(a) forming a bonding pad and an extraction electrode each comprised of an uppermost layer wiring in a product circuit region;

(b) forming a protection film on an upper layer of said uppermost layer wiring; and

(c) partially exposing a surface of said bonding pad by removing a predetermined part of said protection film,

wherein said uppermost layer wiring is formed by depositing a conductive body and then patterning by a lithography method,

a plurality of TEGs provided with said extraction electrode are formed in said product circuit region, and

after partially exposing the surface of said extraction electrode by removing said protection film on said extraction electrode, a probe having a tip radius of curvature of about 0.05 μm to 0.8 μm is contacted to said extraction electrode, and then said TEG is measured.

49. (New) the method of manufacturing a semiconductor device according to claim 48,

wherein said protection film on said extraction electrode is removed by a focused ion beam method or a selective etching method.

50. (New) A method of manufacturing a semiconductor device, comprising the steps of:

(a) forming a bonding pad and an extraction electrode each comprised of an uppermost layer wiring in a product circuit region;

(b) forming a protection film on an upper layer of said uppermost layer wiring; and

(c) partially exposing a surface of said bonding pad by removing a predetermined part of said protection film,

wherein said uppermost layer wiring is formed by depositing a conductive body and then patterning by a lithography method,

a plurality of logic circuits provided with said extraction electrode are formed in said product circuit region, and

after partially exposing the surface of said extraction electrode by removing said protection film on said extraction electrode, a probe having a tip radius of curvature of about 0.05 μm to 0.8 μm is contacted to aid extraction electrode, and then said TEG is measured.

51. (New) The method of manufacturing a semiconductor device according to claim 50;

wherein said protection film on said extraction electrode is removed by a focused ion beam method or a selective etching method.

52. (New) The method of manufacturing a semiconductor device according to claim 50;

wherein said logic circuit comprises n input terminals and m output terminals, and n + m + 3 probes are contacted to said extraction electrodes to evaluate a logic value of said logic circuit.

53. (New) The method of manufacturing a semiconductor device according to claim 52,

wherein one of said probes is a probe for contact confirmation.